University of California, Santa Barbara

Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Final Exam
December 14, 2006

Name _____

Perm # _____

Lab Section _____

Problem #1 (25 points) _____

Problem #2 (25 points) _____

Problem #3 (25 points) _____

Problem #4 (25 points) _____

Total (100 points) _____

- This is a 3 hour exam; closed book, closed notes, no calculators.
- Answer all questions (except timing diagrams) on the paper provided by the instructor; answer timing diagram problems on exam sheet.
- Write on only one side of the paper.
- Attach answer sheets to this exam in the correct order.
- Include your name and perm # on every sheet.

Problem #1.

For the machine defined by the state table below:

PS	X = 0	X = 1	Z
A	H	G	0
B	A	E	1
C	A	A	1
D	G	F	0
E	D	G	0
F	E	A	1
G	C	D	0
H	G	B	0

1. Minimize the machine using an Implication Chart

2. Verify your answer to part 1 above by deriving the equivalence partition (using the Moore reduction procedure).

3. Construct the state table for the reduced machine.

Problem #2.

In this problem you are to design the controller for an electronic black jack game. For those unfamiliar with the game, the object is to draw cards and get as close to 21 as possible without going over. You play against a dealer who also draws cards to 21. Player or dealer with the highest total without going over 21, wins the game.

There are two control inputs, the Deal button (D) and the Stand button (S). There are also inputs indicating that the current total ("active participant") is < 17 H(it), that the current total ("active participant") is > 21 B(ust) and that the player currently has a higher T(otal) than the dealer.

There are only two participants in the game, the dealer and the player, and only one is the "active participant" at any given time. The game begins with the player pressing the deal button (D). The player is the "active participant" in the idle state. Two cards are then dealt to both the player and the dealer. (You can assume the game has a display showing all of the player's cards and one of the dealer's (the dealer's "up card"); this is not part of the controller design).

Based on his total, the player then decides whether to draw more cards in an attempt to get closer to 21 (again, without going over). To draw an additional card, the player presses the deal button (D). If after drawing a card the player's total exceeds 21, the Bust (B) input goes high, the player loses and the game is over. To stop drawing cards (the player is satisfied with his total) and make the dealer the "active participant", the player presses the stand button (S).

If the player has not drawn to a total exceeding 21 and has pressed the stand button (S), control passes to the dealer. The dealer draws cards until his total exceeds 17 (at which time the participant with the higher total wins) or until his total exceeds 21 (at which time the player wins).

The controller has several outputs. The first, I(nitialize), causes 2 cards to be dealt to both the player and the dealer. A second, C(ard), causes a single card to be dealt to the active participant. A third output indicates whether the player or the dealer is currently active, P(layer). A fourth output indicates that the player has just won (W)inner.

Summarizing the inputs and outputs to this machine:

Inputs (maintain the order DSHBT in your solution):

D: Deal Button
S: Stand Button
H: Active participant total < 17
B: Active participant total > 21
T: Player total > dealer total

Outputs (maintain the order ICPW in your solution):

I: Deal 2 cards to both player and dealer
C: Deal single card to active participant
P: Player is currently active participant (0 indicates dealer active)
W: Player has won

1. Construct a state diagram for the controller. Design the controller as a Mealy machine.

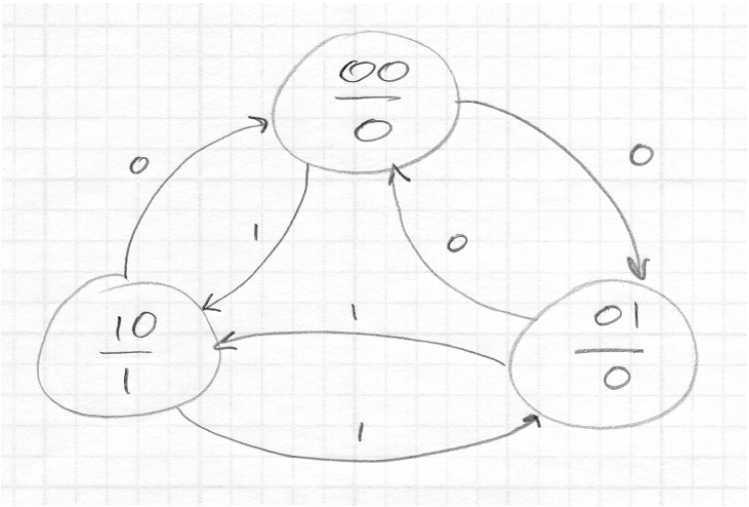
   - You can assume that the D and S inputs won't be active at the same time.
   - You should also assume that state transitions will be triggered by either D or S being pressed or by the indicators H or B becoming active, but never both simultaneously (this simplifies things).
   - You can further assume that D and S are disabled when the dealer is the active participant
   - The assumptions above and the resulting don't care input conditions will

make the state diagram considerably simpler.

You will be graded on both the correctness and simplicity (number of states and number of transitions) of your design.

Problem #3.

For the state diagram shown below (assume the state variables are A and B and that the output Z = A):



1. Construct a state table.

2. Construct next state maps and determine next state equations for A+ and B+.

3. Determine the J and K inputs to the A and B flip flops. Recall the excitation table for the JK flip flop:

Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

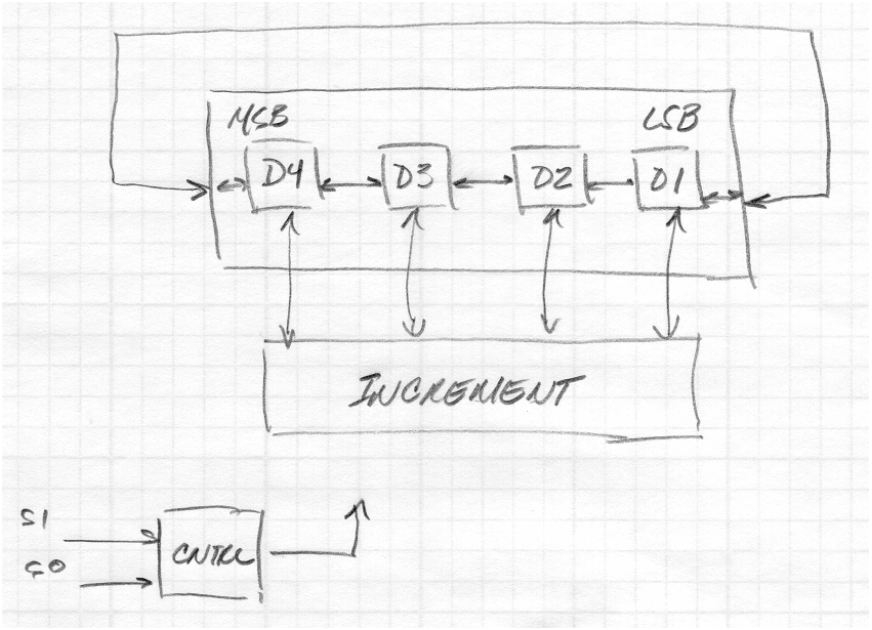
4. The secondary state assignment often determines (in part) the complexity of the machine's implementation. In the state diagram above, the states are arbitrarily assigned the values 00, 01 and 10 (requiring only 3 of the 4 possible state assignments). Because of this secondary state assignment, an input to one of the flip flops includes 2 product terms and a sum term (requiring additional logic)

Can you find a different secondary state assignment that results in the J and K inputs to the A and B flip flops consisting of only the input x (or its complement), the state variables (or their complements) or the constant 1, i.e., no additional logic? The output Z should also remain equal to a state variable or its complement (*ideally* $Z = A$*, as above*). If so, demonstrate the assignment by determining the J and K inputs to the A and B flip flops.

Problem #4

In this problem you are to design a 4-bit register with increment and rotate capabilities using only 7474 D flip-flops, 74157 quad, 2:1 multiplexers and 7482 2-bit, binary full adders.

The register has a 2-bit control input (S1S2) which causes the register to rotate left (S1S0 = 10, LSB ← MSB), rotate right (S1S0 = 01, MSB ← LSB), increment (S1S0 = 11) or do nothing (S1S0 = 00), i.e., hold contents. A block diagram is shown below:



Data Sheets for the three devices follow:

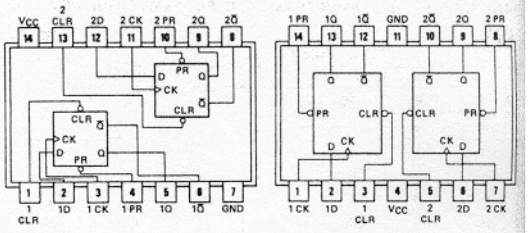
7474

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

74

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$



SN5474 (J)
SN54H74 (J)
SN54L74 (J)
SN54LS74A (J, W)
SN54S74 (J, W)

SN7474 (J, N)
SN74H74 (J, N)
SN74L74 (J, N)
SN74LS74A (J, N)
SN74S74 (J, N)

SN5474 (W)
SN54H74 (W)
SN54L74 (T)

See pages 6-46, 6-50, 6-54, and 6-56

recommended operating conditions

		SERIES 54/74	'70			'72, '73, '76, '107			'74			'109			'110			'111			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		Series 54	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
		Series 74	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}					−400			−800			−400			−800			−800			−800	μA
Low-level output current, I_{OL}					16			16			16			16			16			16	mA
Pulse width, t_w	Clock high		20			20			30			20			25			25			ns
	Clock low		30			47			37			20			25			25			
	Preset or clear low		25			25			30			20			25			25			
Input setup time, t_{su}			20↑			0↑			20↑			10↑			20↑			0↑			ns
Input hold time, t_h			5↑			0↑			5↑			0↑			5↑			30↑			ns
Operating free-air temperature, T_A		Series 54	−55		125	−55		125	−55		125	−55		125	−55		125	−55		125	°C
		Series 74	0		70	0		70	0		70	0		70	0		70	0		70	

↑↓The arrow indicates the edge of the clock pulse used for reference: ↑ for the rising edge, ↓ for the falling edge.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'70			'72, '73 '76, '107			'74			'109			'110			'111			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Note 2	20	35		15	20		15	25		25	33		20	25		20	25		MHz
t_{PLH}	Preset (as applicable)	Q				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		$\bar{Q}$				50		25	40			40		23	35		18	25		21	30	
t_{PLH}	Clear (as applicable)	$\bar{Q}$				50		16	25			25		10	15		12	20		12	18	ns
t_{PHL}		Q				50		25	40			40		17	25		18	25		21	30	
t_{PLH}	Clock	Q or $\bar{Q}$			27	50		16	25		14	25		10	16		20	30		12	17	ns
t_{PHL}					18	50		25	40		20	40		18	28		13	20		20	30	

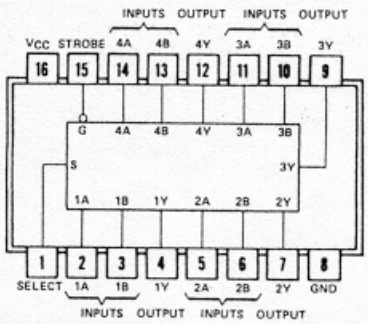
¶f_{max} ≡ maximum clock frequency; t_{PLH} ≡ propagation delay time, low-to-high-level output; t_{PHL} ≡ propagation delay time, high-to-low-level output.

NOTE 2: Load circuit and voltage waveforms are shown on page 3-10.

74157

QUAD 2- TO 1-LINE DATA SELECTORS/MULTIPLEXERS

157 NONINVERTED DATA OUTPUTS



FUNCTION TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	'157, 'L157, 'LS157, 'S157
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

H = high level, L = low level, X = irrelevant

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNI
t_{PLH}	Data	C_L = 15 pF, R_L = 400 Ω, See Note 3		9	14	ns
t_{PHL}				9	14	
t_{PLH}	Strobe			13	20	ns
t_{PHL}				14	21	
t_{PLH}	Select			15	23	ns
t_{PHL}				18	27	

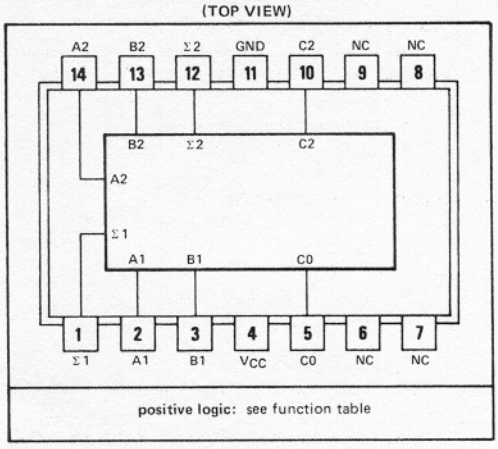
¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 3: Load circuit and voltage waveforms are shown on page 3-10.

7482

TYPES SN5482, SN7482
2-BIT BINARY FULL ADDERS

BULLETIN NO. DL-S 7211836, DECEMBER 1972

SN5482 . . . J OR W PACKAGE
SN7482 . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see function table

NC–No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS					
				WHEN C0 = L			WHEN C0 = H		
A1	B1	A2	B2	Σ1	Σ2	C2	Σ1	Σ2	C2
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see note 4)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C0	Σ1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{PHL}						40	
t_{PLH}	B2	Σ2				40	ns
t_{PHL}						35	
t_{PLH}	C0	Σ2				38	ns
t_{PHL}						42	
t_{PLH}	C0	C2	C_L = 15 pF, R_L = 780 Ω		12	19	ns
t_{PHL}					17	27	

¶t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output
NOTE 4: Load circuit and voltage waveforms are shown on page 3-10.

1. Construct a schematic diagram which implements the least significant bit of the rotate and hold portions of the design.

   Assume the strobe inputs (G) on the 74157's are tied to ground, meaning the MUX's are always enabled. Also assume that the preset and clear inputs to the 7474 D flip flops are tied high, meaning they are always disabled. You needn't worry about initializing the register.

   Based on the above, you only need to include the signals that are used in the design (you don't need to account for every pin on the schematic). Clearly indicate which devices are being used where.

2. What is the critical path (worst case combinational logic delay) in your design? You should assume that the 2-bit control input (S1S0) becomes valid at the same time that the Q outputs of the 7474 D flip flops become valid (synchronous system).

3. What is the minimum clock period (1/maximum frequency) of your design?

4. Add the circuitry necessary to add the increment function. Construct a schematic diagram of the increment circuitry for the two, least significant bits. You don't need to include the rotate/hold circuitry again, but do indicate where it would be added to the design in part 1 above and how it will be cascaded in part 5 below.

5. For the full, 4-bit register (cascaded copies of the design from part 4 above), what is the critical path in your design with the increment function added? Assume that the propagation delay of the adder is the same from any of Ai, Bi or C0 to C2 (carry out), tPLH = 19ns and tPHL = 27ns.

6. What is the new minimum clock period of your design (with the increment function)?